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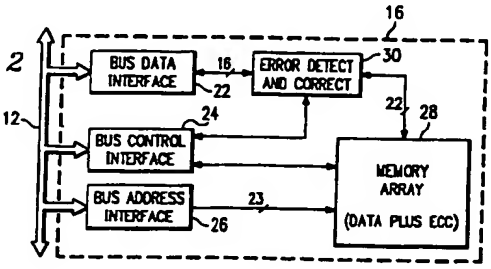
(54) Memory subsystem with error correction.

(57) A memory subsystem is provided which uses memory devices having known bad bits. In order to prevent memory storage errors from occurring in the subsystem, error detection and correction circuitry is also provided. The error detection and correction circuitry is wholly contained within the memory subsystem, and is not visible beyond its boundaries. The error detection and correction circuitry can correct data stored in the array even when one of the bits within the array is permanently nonfunctional. Therefore, although data is incorrectly stored into and read from the array, these errors are corrected, and only accurate data passes beyond the boundaries of the memory subsystem.

FIG. 2



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in the art, the use of 6 error correction bits will allow all single bit errors which occur in data read from the memory array **28** to be corrected. Therefore, 6 error correcting bits are used, so that the error detect and correction circuitry **30** reads and writes 22 bits to the memory array **28**. Commercially available devices can be used to perform the error detecting correction circuitry **30** functions, and one example of such a suitable device is the MB01462 device available from Fujitsu.

According to the present invention, integrated circuit memory chips which are known to have hard bit failures are used to populate the memory array **28**. Hard bit failures for DRAM and SRAM memory devices are generally of the stuck-at-0 or stuck-at-1 type. A completed integrated circuit memory chip which has 1 or more hard bit failures is generally scrapped as nonfunctional, even though most of the bits actually function properly. This is because in previous memory systems, all bits must be functional to ensure proper operation of the system. With the present invention, these devices which were previously considered nonfunctional are used to provide a fully functional memory subsystem at a relatively low cost.

As described above, the error detect and correct circuitry **30** can actually correct for 1 bit errors in data read from the memory array. Therefore, it is important that, for each word which is addressable within the array **28**, no more than 1 hard bit error occurs. This consideration is illustrated in **Figure 3**, in which the memory array **28** is represented logically as 16 columns of data **32**. In addition to the data bits **32**, 6 error correcting bits **34** are also contained within the array.

Figure 3 shows a single addressable entry **36** or row, of the array **28** which contains 22 data bits. For the memory array **28** which uses 23 address bits, there are 2^{23} such entries **36**. For each of these entries **36**, there can be no more than 1 hard bit failure among the 22 bits stored in the array. So long as every entry within the array has no more than 1 hard bit failure, every entry can be completely corrected by the error detect and correct circuitry **30** to provide a fully functional memory subsystem to the remainder of the computer system **10**.

In one possible configuration, each bit position of the data bits **32** is represented by a single memory device. For the 4 megaword memory described above, 4 megabit X 1 memory chips can be used for each bit position, with 22 such memory chips being required. Even if each memory chip used in the array **28** has 1,000 bad bits, there are only approximately 22,000 bad bits in the array. Since there are over 4,000,000 separately addressed entries, the proportion of addressable words **36** which will have one of the bad bits is on the order 1/2 of 1 percent. Assuming that the bad bits are more or less randomly located on the memory chips, the chances that any one entry **36** will have more than 1 bad bit are fairly low. If desired, each of the chips used in the array can be tested prior to use in order to map out the location of bad bits and ensure that no entries have more than 1. Alternatively chips can simply be placed into the array and the entire array tested. Occasionally, some entries will have 2 or more bad bits, and the chips in these arrays can be removed and replaced with other chips. On a statistical basis, most of the time the memory array **28** will be fully functional with the addition of the error detection and correct circuitry **30**.

Since most of the entries within the array **28** are fully functional, the described technique, which uses known nonfunctional parts, actually results in a memory subsystem which is better protected from errors than standard subsystems which use simple parity checks to indicate data errors. More than 99 percent of the entries in the array **28** will typically have no hard bit failures, and the error detection and correct circuitry will allow proper functioning of the memory even if a soft bit failure occurs during normal operation of the system. Thus, unlike typical conventional memory subsystems for microcomputers, more than 99 percent of the memory array is protected from soft errors by the error correction circuitry. The remaining small fraction of the array, already having a hard bit failure within each entry, is no more or less prone to failure than typical memory subsystems which start with fully functional chips and do not use error correction circuitry.

The memory subsystem shown in **Figure 2** is somewhat more complex than a typical 16 bit memory subsystem for a microcomputer. This is because of the additional cost and complexity of the error detect and correction circuitry **30** and the requirement for extra error correction bits **34**. Since a typical microcomputer subsystem uses 1 parity bit for each 8 data bits, the subsystem described above requires an extra 4 bit positions memory array **28**. However, the overall cost for the memory subsystem described above can be cost competitive with available prior art systems. With a conventional memory subsystem, the cost of 18 high density memory chips is a major factor in the overall cost of the device. With the system described above, the nonfunctional memory chips are obtainable at a nominal cost, with the extra expense of the error detect and correction circuitry **30** contributing to the overall cost of the device. In both cases, the interface circuitry to the system bus is the same. Therefore, if a single 16 bit error detection and correction circuit **30** can be obtained for significantly less cost than 18 high density

means for addressing said memory array;

means for providing to be written into said array; and

error correcting means for storing error correction data into said array, and for using such error correction data to correct errors in data read from said array.

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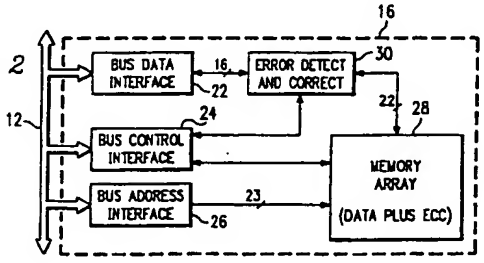

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